GPI WEB CLIENT

Help | Comments | Logout

Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers

Search Results - *6 Hits.*

Term	Occurrence
L11 AND L23	6

Database: US Patents
Japanese Patents
European Patents
USOCR Patents

Refine Search:
l11 and l23

Search History

DB Name	Query	Hit Count	Set Name	Time
USPAT	l11 and l23	6	L24	Mon Mar 29 16:50:02 1999
USPAT	locked/BI 0W loop/BI	13315	L23	Mon Mar 29 16:49:26 1999
USPAT	l16 and l11	1	L22	Mon Mar 29 16:48:47 1999
USPAT	l13 and l14 and l11	10	L21	Mon Mar 29 16:48:30 1999
USPAT	l13 and l14	1110	L20	Mon Mar 29 16:48:12 1999
USPAT	l13 and l14 and l16	0	L19	Mon Mar 29 16:48:05 1999
USPAT	l13 and l14 and l16	0	L18	Mon Mar 29 16:47:26 1999
USPAT	l13 and l14 and l15	0	L17	Mon Mar 29 16:47:16 1999
USPAT	delay 0W locked/BI 0W loop/BI	177	L16	Mon Mar 29 16:45:46 1999

USPAT	delay/BI 0W locked/BI	208	L15	Mon Mar 29 16:45:08 1999
USPAT	echo 0P (clock or timer or timing)/BI	2585	L14	Mon Mar 29 16:44:32 1999
USPAT	digital 0P (clock or timer or timing)/BI	59404	L13	Mon Mar 29 16:43:18 1999
USPAT	l9 and l6	0	L12	Mon Mar 29 16:41:51 1999
USPAT	l9 and (l8 or l7)	54	L11	Mon Mar 29 16:41:33 1999
USPAT	l7 and (l8 or l9)	161	L10	Mon Mar 29 16:40:55 1999
USPAT	l1 and l2 and l4	172	L9	Mon Mar 29 16:39:51 1999
USPAT	digital and adjust and controller	15952	L8	Mon Mar 29 16:39:20 1999
USPAT	digital and vernier and controller	319	L7	Mon Mar 29 16:38:52 1999
USPAT	digital and vernier and controller and adjust	161	L6	Mon Mar 29 16:38:31 1999
USPAT	digital and vernier and controller and adjust and synchronize	37	L5	Mon Mar 29 16:37:05 1999
USPAT	(phase or delay)/BI 0P (clock or timer or timing)/BI	85211	L4	Mon Mar 29 16:36:12 1999
USPAT	(phase or delay)/BI AND (clock or timer or timing)/BI	158069	L3	Mon Mar 29 16:35:10 1999
USPAT	memory/BI 0W controller/BI	5170	L2	Mon Mar 29 16:32:46 1999
USPAT	synchronize/BI 0P memory/BI	2866	L1	Mon Mar 29 16:31:33 1999

Z39.50 Gateway Based on **CNIDR** Isite

L 21

GPI WEB CLIENT

Help | Comments | Logout

Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers

Search Results - *Records 1 through 10 of 10 returned.*

Generate Collection

1. 5,867,501, Feb. 2, 1999, Encoding for communicating data and commands; Robert W. Horst, et al., 370/474 [IMAGE AVAILABLE]

1. ☐ Abstract | Bkgnd/Summ | Clms | Draw. Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

2. 5,838,894, Nov. 17, 1998, Logical, fail-functional, dual central processor units formed from three processor units; Robert W. Horst, 709/239; 714/12 [IMAGE AVAILABLE]

2. ☐ Abstract | Bkgnd/Summ | Clms | Draw. Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

3. 5,790,776, Aug. 4, 1998, Apparatus for detecting divergence between a pair of duplexed, synchronized processor elements; David Paul Sonnier, et al., 710/18, 32, 61; 714/12 [IMAGE AVAILABLE]

3. ☐ Abstract | Bkgnd/Summ | Clms | Draw. Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

4. 5,751,955, May 12, 1998, Method of synchronizing a pair of central processor units for duplex, lock-step operation by copying data into a corresponding locations of another memory; David Paul Sonnier, et al., 709/400; 712/43; 714/11 [IMAGE AVAILABLE]

4. ☐ Abstract | Bkgnd/Summ | Clms | Draw. Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

5. 5,751,932, May 12, 1998, Fail-fast, fail-functional, fault-tolerant multiprocessor system; Robert W. Horst, et al. [IMAGE AVAILABLE]

5. ☐ Abstract | Bkgnd/Summ | Clms | Draw. Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

6. 5,689,689, Nov. 18, 1997, Clock circuits for synchronized processor systems having clock generator circuit with a voltage control oscillator producing a clock signal synchronous with a master clock signal; Steven C. Meyers, et al., 395/553, 500; 713/400, 500 [IMAGE AVAILABLE]

6. ☐ Abstract | Bkgnd/Summ | Clms | Draw. Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

7. 5,675,807, Oct. 7, 1997, Interrupt message delivery identified by storage location of received interrupt data; Geoffrey I. Iswandhi, et al., 710/260, 4, 263, 268, 269; 714/48 [IMAGE AVAILABLE]

7. ☐ Abstract | Bkgnd/Summ | Clms | Draw. Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

8. 5,675,579, Oct. 7, 1997, Method for verifying responses to messages using a barrier message; William Joel Watson, et al., 370/248, 241; 709/237; 714/43 [IMAGE AVAILABLE]

8. ☐ Abstract | Bkgnd/Summ | Clms | Draw. Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

9. 5,574,849, Nov. 12, 1996, Synchronized data transmission between elements of a processing system; David P. Sonnier, et al. [IMAGE AVAILABLE]

9. ☐ Abstract | Bkgnd/Summ | Clms | Draw. Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

10. 4,347,618, Aug. 31, 1982, Apparatus for processing weather radar information; Stephen P. Kavouras, et al., 375/259; 342/26; 348/442; 455/9; 702/3 [IMAGE AVAILABLE]

10. ☐ Abstract | Bkgnd/Summ | Clms | Draw. Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

Generate Collection

L21

USPAT

Term	Occurrence
L13 AND L14 AND L11	10
DIGITAL/BI	232134
CLOCK/BI	150006
TIMER/BI	80396
TIMING/BI	212098
DIGITAL/BI (0P) (CLOCK/BI OR TIMER/BI OR TIMING/BI)	59404
ECHO/BI	14464
CLOCK/BI	150006
TIMER/BI	80396
TIMING/BI	212098
ECHO/BI (0P) (CLOCK/BI OR TIMER/BI OR TIMING/BI)	2585
SYNCHRONIZE/BI	26009
MEMORY/BI	250962
SYNCHRONIZE/BI (0P) MEMORY/BI	2866
MEMORY/BI	250962
CONTROLLER/BI	168863
MEMORY/BI (0W) CONTROLLER/BI	5170
PHASE/BI	478837
DELAY/BI	193043
CLOCK/BI	150006
TIMER/BI	80396
TIMING/BI	212098
(PHASE/BI OR DELAY/BI) (0P) (CLOCK/BI OR TIMER/BI OR TIMING/BI)	85211
DIGITAL/BI	232134
ADJUST/BI	246420
CONTROLLER/BI	168863
DIGITAL/BI	232134
VERNIER/BI	3540
CONTROLLER/BI	168863

Show 10 More Patents Starting At: 1 Display Format: B

Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers

Help | Comments | Logout

Z39.50 Gateway Based on **CNIDR** Isite

L22

GPI WEB CLIENT

Help | Comments | Logout

Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers

Search Results - *Record 1 of 1 returned.*

Generate Collection

1. 5,623,644, Apr. 22, 1997, Point-to-point phase-tolerant communication; Keith-Michael W. Self, et al., 709/234; 710/29, 52 [IMAGE AVAILABLE]

1. ☐ Abstract | Bkgnd/Summ | Clms | Draw. Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

Generate Collection

USPAT

Term	Occurrence
L16 AND L11	1
DELAY/BI	193043
LOCKED/BI	187655
LOOP/BI	224006
DELAY/BI (0W) LOCKED/BI (0W) LOOP/BI	177
SYNCHRONIZE/BI	26009
MEMORY/BI	250962
SYNCHRONIZE/BI (0P) MEMORY/BI	2866
MEMORY/BI	250962
CONTROLLER/BI	168863
MEMORY/BI (0W) CONTROLLER/BI	5170
PHASE/BI	478837
DELAY/BI	193043
CLOCK/BI	150006
TIMER/BI	80396
TIMING/BI	212098
(PHASE/BI OR DELAY/BI) (0P) (CLOCK/BI OR TIMER/BI OR TIMING/BI)	85211
DIGITAL/BI	232134
ADJUST/BI	246420
CONTROLLER/BI	168863
DIGITAL/BI	232134
VERNIER/BI	3540
CONTROLLER/BI	168863

Show 10 More Patents Starting At: 1 Display Format: B

Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers

Help | Comments | Logout

L24

GPI WEB CLIENT

Help | Comments | Logout

Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers

Search Results - *Records 1 through 6 of 6 returned.*

Generate Collection

1. 5,657,457, Aug. 12, 1997, Method and apparatus for eliminating bus contention among multiple drivers without performance degradation; Darius D. Gaskins, 710/107; 364/271, 271.2, 271.5, DIG.1 [IMAGE AVAILABLE]

1. ☐ Abstract | Bkgnd/Summ | Clms | Draw. Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

2. 5,623,644, Apr. 22, 1997, Point-to-point phase-tolerant communication; Keith-Michael W. Self, et al., 709/234; 710/29, 52 [IMAGE AVAILABLE]

2. ☐ Abstract | Bkgnd/Summ | Clms | Draw. Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

3. 5,550,594, Aug. 27, 1996, Apparatus and method for synchronizing asynchronous signals; J. Carl Cooper, et al., 348/513, 512 [IMAGE AVAILABLE]

3. ☐ Abstract | Bkgnd/Summ | Clms | Draw. Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

4. 5,416,510, May 16, 1995, Camera **controller** for stereoscopic video system; Lenny Lipton, et al., 348/43, 386, 717 [IMAGE AVAILABLE]

4. ☐ Abstract | Bkgnd/Summ | Clms | Draw. Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

5. 5,347,559, Sep. 13, 1994, Apparatus and method of data transfer between systems using different clocks; Thomas B. Hawkins, et al., 377/54, 56; 713/502, 601 [IMAGE AVAILABLE]

5. ☐ Abstract | Bkgnd/Summ | Clms | Draw. Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

6. 4,347,618, Aug. 31, 1982, Apparatus for processing weather radar information; Stephen P. Kavouras, et al., 375/259; 342/26; 348/442; 455/9; 702/3 [IMAGE AVAILABLE]

6. ☐ Abstract | Bkend/Summ | Clms | Draw Desc | Front | Full | KWIC | Legal | Refs | Cit | Cls | Image

Generate Collection

USPAT

Term	Occurrence
L11 AND L23	6
SYNCHRONIZE/BI	26009
MEMORY/BI	250962
SYNCHRONIZE/BI (0P) MEMORY/BI	2866
MEMORY/BI	250962
CONTROLLER/BI	168863
MEMORY/BI (0W) CONTROLLER/BI	5170
PHASE/BI	478837
DELAY/BI	193043
CLOCK/BI	150006
TIMER/BI	80396
TIMING/BI	212098
(PHASE/BI OR DELAY/BI) (0P) (CLOCK/BI OR TIMER/BI OR TIMING/BI)	85211
DIGITAL/BI	232134
ADJUST/BI	246420
CONTROLLER/BI	168863
DIGITAL/BI	232134
VERNIER/BI	3540
CONTROLLER/BI	168863
LOCKED/BI	187655
LOOP/BI	224006
LOCKED/BI (0W) LOOP/BI	13315

Show 10 More Patents Starting At: 1 Display Format: B

Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers

Help | Comments | Logout

L24

Z39.50 Gateway Based on **CNIDR** Isite

THIS PAGE BLANK